

## AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application:

### Listing of Claims:

- 1           1. (Currently amended) A method for matching speeds of asynchronous  
2           operation between a local chip and a neighboring chip, the method comprising:  
3           deriving an internal frequency signal from an internal oscillator on the  
4           local chip;  
5           receiving an external frequency signal from a neighboring chip;  
6           comparing the internal frequency signal with the external frequency signal  
7           to generate a control signal;  
8           adjusting the operating speed of the local chip by applying the control  
9           signal to the internal oscillator ; and  
10          wherein if the internal frequency signal is faster than the external  
11          frequency signal, the control signal causes the internal frequency signal to slow  
12          down;  
13          wherein the neighboring chip similarly adjusts the external frequency  
14          signal with respect to the internal frequency signal so that the local chip and the  
15          neighboring chip operate at a substantially maximum common frequency; and  
16          ~~generating a substantially maximum common frequency to be used by the~~  
17          ~~local chip and the neighboring chip by coupling circuitry within the local chip and~~  
18          ~~circuitry within the neighboring chip to generate an asynchronous control loop~~  
19          ~~which generates the substantially maximum common frequency;~~

20        wherein ~~circuitry in~~ the local chip and ~~circuitry in~~ the neighboring chip are  
21        coupled together ~~in to form~~ an asynchronous control loop, which ~~generates a~~  
22        determines the substantially maximum common frequency without reference to an  
23        external synchronous clock signal.

1            2 (Canceled).

1            3. (Previously presented) The method of claim 1, wherein receiving the  
2        external frequency signal from the neighboring chip involves receiving the  
3        external frequency signal through a capacitor, an inductor, a resistor, a  
4        transmission line, or a direct contact.

1            4. (Original) The method of claim 1, wherein comparing the internal  
2        frequency signal with the external frequency signal involves converting the  
3        internal frequency signal and external frequency signal into corresponding current  
4        or voltage signals, which are proportional to the frequencies of the frequency  
5        signals.

1            5. (Original) The method of claim 4,  
2        wherein the internal frequency signal and the external frequency signal are  
3        converted into corresponding current signals;

4            wherein comparing the internal frequency signal with the external  
5        frequency signal involves comparing the two current signals to generate a  
6        difference current signal; and

7            wherein the method further comprises:

8            coupling the difference current signal to an integrating capacitor to  
9        produce an integrated voltage signal;

10                   applying an offset current source to the integrating capacitor to  
11           compensate for transistor leakages, parasitics, and/or nonlinearities; and  
12                   coupling the integrating capacitor to an amplifier, wherein the  
13           input to the amplifier is the integrated voltage signal and the output of the  
14           amplifier is the control signal.

1           6. (Original) The method of claim 1, further comprising filtering the  
2   control signal to improve matching between the local chip's operating speed and  
3   the neighboring chip's operating speed.

1           7. (Original) The method of claim 6, wherein filtering the control signal  
2   involves coupling a filter capacitor between the control signal and ground.

1           8. (Previously presented) The method of claim 1, wherein  
2           the internal frequency signal has a frequency that is a fraction of the  
3   internal oscillator frequency of the local chip; and wherein  
4           the external frequency signal has a frequency that is a fraction of an  
5   external oscillator frequency of the neighboring chip.

1           9. (Currently amended) An apparatus for matching speeds of asynchronous  
2   operation between a local chip and a neighboring chip, the apparatus comprising:  
3           an internal oscillator on the local chip, from which an internal frequency  
4   signal can be derived;  
5           a receiving mechanism configured to receive an external frequency signal  
6   from a neighboring chip;  
7           a comparison mechanism configured to compare the internal frequency  
8   signal with the external frequency signal to generate a control signal; and

9 an adjusting mechanism configured to adjust the operating speed of the  
10 local chip and the internal oscillator by applying the control signal to the internal  
11 oscillator;

12 wherein if the internal frequency signal is faster than the external  
13 frequency signal, the control signal causes the internal frequency signal to slow  
14 down;

15 wherein the neighboring chip similarly adjusts the external frequency  
16 signal with respect to the internal frequency signal so that the local chip and the  
17 neighboring chip operate at a substantially maximum common frequency; and

18 ~~a generating mechanism configured to generate a substantially maximum~~  
19 ~~common frequency to be used by the local chip and the neighboring chip by~~  
20 ~~coupling circuitry within the local chip and circuitry within the neighboring chip~~  
21 ~~to generate an asynchronous control loop which generates the substantially~~  
22 ~~maximum common frequency;~~

23 wherein ~~circuitry in~~ the local chip and ~~circuitry in~~ the neighboring chip are  
24 coupled together ~~in to form~~ an asynchronous control loop, which ~~generates a~~  
25 ~~determines the~~ substantially maximum common frequency without reference to an  
26 external synchronous clock signal.

1 10 (Canceled).

1 11. (Original) The apparatus of claim 9, wherein the receiving mechanism  
2 is configured to receive the external frequency signal from the neighboring chip  
3 through a capacitor, and inductor, a resistor, a transmission line, or a direct  
4 contact.

1 12. (Original) The apparatus of claim 9, wherein the comparison  
2 mechanism is configured to convert the internal frequency signal and the external

3 frequency signal into corresponding current or voltage signals, which are  
4 proportional to the frequencies of the frequency signals.

1 13. (Original) The apparatus of claim 12,  
2 wherein the external frequency signal and the internal frequency signal are  
3 converted into corresponding current signals;  
4 wherein the comparison mechanism is configured to compare the two  
5 current signals to generate a difference current signal; and  
6 wherein the apparatus further comprises:  
7 an integrating capacitor to which the difference current signal is  
8 coupled to produce an integrated voltage signal;  
9 an offset current source applied to the integrating capacitor to  
10 compensate for transistor leakages, parasitics, and/or nonlinearities; and  
11 an amplifier to which the integrating capacitor is coupled, wherein  
12 the input to the amplifier is the integrated voltage signal and the output of  
13 the amplifier is the control signal.

1 14. (Original) The apparatus of claim 9, further comprising a filtering  
2 mechanism configured to filter the control signal to improve matching between  
3 the local chip's operating speed and the neighboring chip's operating speed.

1 15. (Original) The apparatus of claim 14, wherein the filtering mechanism  
2 includes a filter capacitor coupled between the control signal and ground.

1 16. (Previously presented) The apparatus of claim 9, wherein  
2 the internal frequency signal has a frequency that is a fraction of the  
3 internal oscillator frequency of the local chip; and wherein

4 the external frequency signal has a frequency that is a fraction of an  
5 external oscillator frequency of the neighboring chip.

1 17. (Currently amended) A computer system that includes a circuit for  
2 matching speeds of asynchronous operation between a local chip and a  
3 neighboring chip, the circuit comprising:

4 a central processing unit;

5 a semiconductor memory;

6 an internal oscillator circuit on the local chip, from which an internal  
7 frequency signal can be derived;

8 a receiver circuit for receiving an external frequency signal from a  
9 neighboring chip;

10 a comparison circuit for comparing the internal frequency signal with the  
11 external frequency signal to generate a control signal; and

12 an adjustment circuit for adjusting the operating speed of the local chip  
13 and the internal oscillator by applying the control signal to and the internal  
14 oscillator;

15 wherein if the internal frequency signal is faster than the external  
16 frequency signal, the control signal causes the internal frequency signal to slow  
17 down;

18 wherein the neighboring chip similarly adjusts the external frequency  
19 signal with respect to the internal frequency signal so that the local chip and the  
20 neighboring chip operate at a substantially maximum common frequency; and

21 ~~a generator circuit for generating a substantially maximum common~~  
22 ~~frequency to be used by the local chip and the neighboring chip by coupling~~  
23 ~~circuitry within the local chip and circuitry within the neighboring chip to~~  
24 ~~generate an asynchronous control loop which generates the substantially~~  
25 ~~maximum common frequency;~~

26        wherein ~~circuitry in~~ the local chip and ~~circuitry in~~ the neighboring chip are  
27        coupled together ~~in to form~~ an asynchronous control loop, which ~~generates a~~  
28        determines the substantially maximum common frequency without reference to an  
29        external synchronous clock signal.

1            18 (Canceled).

1            19. (Original) The computer system of claim 17, wherein the receiver  
2        circuit is configured to receive the external frequency signal from the neighboring  
3        chip through a capacitor, and inductor, a resistor, a transmission line, or a direct  
4        contact.

1            20. (Original) The computer system of claim 17, wherein the comparison  
2        circuit is configured to convert the internal frequency signal and the external  
3        frequency signal into corresponding current or voltage signals, which are  
4        proportional to the frequencies of the frequency signals.

1            21. (Original) The computer system of claim 20,  
2        wherein the external frequency signal and the internal frequency signal are  
3        converted into corresponding current signals;  
4        wherein the comparison circuit is configured to compare the two current  
5        signals to generate a difference current signal; and  
6        wherein the computer system further comprises:  
7            an integrating capacitor to which the difference current signal is  
8            coupled to produce an integral voltage signal;  
9            an offset current source applied to the integrating capacitor to  
10        compensate for transistor leakages, parasitics, and/or nonlinearities; and

11                    an amplifier to which the integrating capacitor is coupled, wherein  
12                    the input to the amplifier is the integral voltage signal and the output of the  
13                    amplifier is the control signal.

1                    22. (Original) The computer system of claim 17, further comprising a  
2                    filtering circuit for filtering the control signal to improve matching between the  
3                    local chip's operating speed and the neighboring chip's operating speed.

1                    23. (Original) The computer system of claim 22, wherein the filter circuit  
2                    includes a filter capacitor coupled between the control signal and ground.

1                    24. (Previously presented) The computer system of claim 17, wherein  
2                    the internal frequency signal has a frequency that is a fraction of the  
3                    internal oscillator frequency of the local chip; and wherein  
4                    the external frequency signal has a frequency that is a fraction of an  
5                    external oscillator frequency of the neighboring chip.

1                    25. (Previously presented) The method of claim 1, wherein adjusting the  
2                    frequency of the local chip involves changing the power-supply voltage of the  
3                    local chip.

1                    26. (Previously presented) The apparatus of claim 9, wherein the adjusting  
2                    mechanism is configured to adjust the frequency of the local chip by changing the  
3                    power-supply voltage of the local chip.

1                    27. (Previously presented) the computer system of claim 17, wherein the  
2                    adjustment circuit is configured to adjust the frequency of the local chip by  
3                    changing the power-supply voltage of the local chip.